CLAIMS

What is claimed is:

1	1. A microelectronic device, comprising:
2	a microelectronic die having an active surface, a back surface, and at least one
3	side;
4	said at least one microelectronic die side comprising at least one beveled sidewall
5	and at least one channel sidewall, wherein said at least one beveled sidewall extends
6	between said channel sidewall and said microelectronic die back surface; and
7	a metallization layer disposed on said microelectronic die back surface and said at
8	least one beveled sidewall.
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- 1 2. The microelectronic device of claim 1, wherein said at least one beveled 2 sidewall is between about 30 degrees and about 60 degrees from said at least one channel 3 sidewall.
- 1 3. The microelectronic device of claim 2, wherein said at least one beveled 2 sidewall is about 45 degrees from said at least one channel sidewall.
- 1 4. The microelectronic device of claim 1, wherein said metallization layer is 2 at least one metal selected from the group consisting of gold, silver, chromium, titanium, 3 nickel vanadium, and nickel.

1	5. A microelectronic device assembly, comprising:
2	a microelectronic die having an active surface, a back surface, and at least one
3	side;
4	said at least one microelectronic die side comprising at least one beveled sidewall
5	and at least one channel sidewall, wherein said at least one beveled sidewall extends
6	between said channel sidewall and said microelectronic die back surface;
7	a metallization layer disposed on said microelectronic die back surface and said at
8	least one beveled sidewall; and
9	a heat dissipation device attached to said microelectronic die back surface with a
10	thermal interface material.
1	6. The microelectronic device of claim 5, wherein said at least one beveled
2	sidewall is between about 30 degrees and about 60 degrees from said at least one channel
3	sidewall.
1	7. The microelectronic device of claim 6, wherein said at least one beveled
2	sidewall is about 45 degrees from said at least one channel sidewall.

- The microelectronic device assembly of claim 5, wherein said 8. 1
- metallization layer is at least one metal selected from the group consisting of gold, silver, 2
- chromium, titanium, tungsten, vanadium, and nickel. 3

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1	9. The microelectronic device assembly of claim 5, wherein said the	ermal
2	interface material is selected from the group consisting of lead, tin, indium, silve	er,
3	copper, and alloys thereof.	

- 1 10. The microelectronic device assembly of claim 5, wherein at least a portion 2 of a fillet of said thermal interface material extend from said metallization layer on said 3 microelectronic die beveled sidewall to said heat dissipation device.
 - 11. A method of dicing a microelectronic device wafer, comprising:

 providing a microelectronic device wafer comprising a semiconductor wafer

 having a back surface, said microelectronic device including at least two integrated

 circuit areas formed therein separated by at least one scribe street;

forming at least one substantially V-shaped notch opposing said at least one scribe street and extending from said semiconductor wafer back surface into said semiconductor wafer, wherein said substantially v-shaped notch comprises at least two sidewalls that terminate at an intersection location;

forming a metallization layer on said semiconductor wafer back surface and said at least two notch sidewalls; and

forming a channel within said at least one scribe street and extending through said interconnection layer, said semiconductor wafer, and said intersection location.

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1	12. The method of claim 11, wherein providing said microelectronic further
2	includes providing said microelectronic device wafer having an interconnection layer
3	disposed on said active surface.

- 1 13. The method of claim 11, wherein forming said substantially v-shaped
 2 notch comprises forming said substantially v-shaped notch by a method selected from the
 3 group consisting of laser ablation, etching, and cutting with a wafer saw.
 - 14. The method of claim 11, wherein forming said metallization layer on said semiconductor wafer back surface and said at least two notch sidewalls comprises depositing at least one layer of metal selected from the group consisting of gold, silver, chromium, titanium, tungsten, vanadium, and nickel.
 - 15. A method of fabricating a microelectronic device assembly, comprising: providing a microelectronic die having an active surface, a back surface, and at least one side, wherein said at least one microelectronic die side comprises at least one beveled sidewall and at least one channel sidewall;
 - disposing a metallization layer on said microelectronic die back surface and said at least one beveled sidewall; and
 - attaching a heat dissipation device to said microelectronic die back surface with a thermal interface material.

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- 1 16. The method of claim 15, wherein disposing said metallization layer
 2 comprises disposing at least one metal selected from the group consisting of gold, silver,
 3 chromium, titanium, tungsten, vanadium, and nickel on said microelectronic die back
 4 surface and said at least one beveled sidewall.
- 1 17. The method of claim 15, wherein attaching said heat dissipation device 2 comprises attaching said heat dissipation device with a thermal interface material selected 3 from the group consisting of lead, tin, indium, silver, copper, and alloys thereof.
 - 18. The method of claim 15, wherein attaching said heat dissipation device comprises attaching said heat dissipation device with said thermal interface material such that a portion of a fillet of said thermal interface material extends from said metallization layer on said at least one beveled sidewall to said heat dissipation device.
 - 1 19. The method of claim 15, wherein providing said microelectronic die comprises:
 - providing a microelectronic device wafer comprising a semiconductor wafer

 having a back surface, said microelectronic device including at least two integrated

 circuit areas formed therein separated by at least one scribe street;
 - forming at least one substantially V-shaped notch opposing said at least one scribe
 street and extending from said semiconductor wafer back surface into said semiconductor

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- wafer, wherein said substantially v-shaped notch comprises at least two sidewalls that
 terminate at an intersection location;
- forming a metallization layer on said semiconductor wafer back surface and said at least two notch sidewalls; and
- forming a channel within said at least one scribe street and extending through said interconnection layer, said semiconductor wafer, and said intersection location.
 - 1 20. The method of claim 19, wherein providing said microelectronic die 2 further includes providing said microelectronic device wafer having an interconnection 3 layer disposed on said active surface.
 - 21. The method of claim 19, wherein forming said substantially v-shaped notch comprises forming said substantially v-shaped notch by a method selected from the group consisting of laser ablation, etching, and cutting with a wafer saw.
 - 1 22. The method of claim 19, wherein forming said metallization layer on said
 2 semiconductor wafer back surface comprises depositing at least one layer of metal
 3 selected from the group consisting of gold, silver, chromium, titanium, tungsten,
 4 vanadium, and nickel.